Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec – 2017**

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| **Code :** | **14EC2001** | **Duration :** | **3hrs** |
| **Sub. Name :** | **DIGITAL ELECTRONICS** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | | **Marks** | |
| 1. | a. | Draw logic diagram and truth table for the Boolean expression given  Q=AB+AC' | | CO1 | 6 |
| b. | Simplify the given Boolean function using k-map  F (a,b,c,d) = Σ (7,13,14,15) | | CO1 | 6 |
| c. | Convert the following  i. (439.25)10 = (-----------)2 ii. (ABC.2)16 = (----------)2 iii. (123)8 = (-----------)2 | | CO1 | 6 |
| d. | Consider a four bit digital to analog converter. The analog value corresponding to digital signals of value 0000 and 0001 are 0 volts 0.0625 volts respectively. The analog value (in volts) corresponding to the digital value 1111 is \_\_\_\_\_\_\_ | | CO1 | 2 |
| (OR) | | | | | |
| 2. | a. | Simplify the following using K map  F (a,b,c,d) = ∑ m (1,3,7,11,15) + d (0,2,5). | | CO1 | 6 |
| b. | Simplify the following using Boolean algebra | | CO1 | 6 |
| c. | Convert the following binary code into gray code  111100 = ------------  Convert the following gray code into binary code  101011 = ------------  Convert the following BCD code into Excess 3 code  1001 = --------------  Give the equivalent BCD code for 16 -------------------- | | CO1 | 8 |
|  |  |  | |  |  |
| 3. | a. | Convert (250.5)10 to base 4. | | CO1 | 6 |
|  | b. | Convert the following expression into canonical form  F(A,B,C) = (A+B) . (A+C) | | CO1 | 4 |
|  | c. | Simplify the following equation using Quine-Mc-Cluskey method  F(a,b,c,d)=Σ (0,1,2,8,10,11,14,15) | | CO1 | 10 |
| (OR) | | | | | |
| 4. | a. | Design a look ahead carry generator circuit with neat diagram. | | CO2 | 10 |
|  | b. | Design a Full subtractor circuit. | | CO2 | 6 |
|  | c. | Implement the following Boolean expression with exclusive-OR and AND gates and draw the logic diagram.  F=AB’CD’+A’BCD’+AB’C’D+A’BC’D | | CO1 | 4 |
|  |  |  | |  |  |
| 5. | a. | Design a Combinational Circuit that compares the magnitude of two inputs, each of two bits wide. | | CO2 | 10 |
|  | b. | Implement the sum of full adder circuit using MUX | | CO2 | 4 |
|  | c. | In the circuit shown in figure , if C = 0, the expression for Y is \_\_\_\_\_\_\_. Justify the same.     1. Y = A + B 2. Y = 3. Y = AB | | CO3 | 6 |
| (OR) | | | | | |
| 6. | a. | Implement the expression AB+C using NAND gate. | | CO1 | 4 |
|  | b. | Design a MOD 5 counter with unused states using T flip-flop. | | CO2 | 6 |
|  | c. | Design a Parallel in Serial out shift register and explain its operation with a neat timing diagram. | | CO2 | 10 |
|  |  |  | |  |  |
| 7. | a. | With sequence table and diagram explain Johnson counter. | | CO2 | 5 |
|  | b. | Design a 3 bit synchronous binary up-down binary using T flip flop. | | CO2 | 10 |
|  | c. | Design a 3 bit odd parity generator circuit. | | CO2 | 5 |
| (OR) | | | | | |
| 8. | a. | With state diagram differentiate between Moore and Mealy Machine. | | CO2 | 6 |
|  | b. | Design the state table, state reduction table and implement the following state diagram using T Flip Flop. | | CO2 | 14 |
|  | | **Compulsory**: | |  |  |
| 9. | a. | With neat timing diagram, explain about 4 bit binary ripple counter | | CO2 | 8 |
|  | b. | Design NAND and NOR gate using CMOS logic Families. | | CO3 | 6 |
|  | c. | Find minimum SoP for the following PoS and implement using PLA F(A,B,C,D) = π (3,4,6,7,11,12,13,14,15) | | CO3 | 6 |

ALL THE BEST